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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,367	06/28/2000	Feng Chen	042390.P8530	6023

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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,367	CHEN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7 and 10-24* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 5, the recitation " a first and a second inverter...and an inverted output terminal of said p-type sense amp." on lines 2-6 is indefinite because it is misdescriptive. According to figure 5, the first inverter (520) and the second inverter (530), each has an input and an output and the "pull-up and a pull down terminal" are not parts of these inverters. Figure 5 shows that the pull-up transistor (540) is connected to the **output** of inverter (520) and the pull-down transistor (570) is connected to the **input** of inverter (520). The same analysis is true for inverter (530). The recitation "said output terminals" in line 5 does not have antecedent basis. The recitation "said pull-down terminals being respectively coupled to a non-inverted output terminal" on line 4-5 is indefinite because as mention above, the "said pull-down terminals" do not exist. The "said pull-down terminals" are actually the input terminals of the first and second inverters (520, 530). The recitation "a third inverter having an input terminal...said pull-up terminal of said first inverter" in lines 10-12 is indefinite because it is misdescriptive. Assume that the "a third inverter" is the left side inverter of the latch (590), the output terminal of this inverter is connected to the output of the first inverter (520), not the "said pull-up terminal" of said first inverter. The same analysis is true for the recitation "said pull-up terminal" in line 12.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 3-6 and 11-16 are rejected under 35 U.S.C.102 (e) as being anticipated by Takahashi (US Pat. 6037,824).

Regarding claim 1, figure 7 of Takahashi shows a circuit comprising: a differential sense circuit (210, 220, 231), a latch (IN1, IN3, IN4, N33-N35) said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle, wherein said differential sense circuit is coupled to said latch in a push-pull (P31, N31, P32, N32). Note that it is inherent that the latch stores "an electronic signal" for at least on clock cycle (iclkb3 or CLOCK CLK of figure 3).

Regarding claim 3, the circuit further comprises a sense amp (210, 220, 231), said sense amp and said differential sense latch. The differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch

Regarding claim 4, the sense amplifier is a P-type amplifier (P11, P12, P13, N12, N13).

Regarding claim 5, the differential sense circuit comprises a first inverter (P31, N31), the second inverter (P32, N32), the third inverter (IN3) and the fourth inverter (IN4).

Regarding claim 6, the differential sense circuit is symmetrical, thus the loads, in operation, are substantially equivalent.

Regarding claim 10, the domino circuit is (P21, N21, P22, N22).

Regarding claims 11 and 12, figure 7 of Katahashi (6,037,824) shows a method for storing electronic signals produced by a differential circuit comprising: pre-charging said differential circuit (elements N12, N13); evaluating said differential circuit (231); sensing differential output signals via a differential sense circuit (231), wherein said differential sense circuit is coupled to a latch (IN1, IN3, IN4, N33-N35) in a push-pull configuration (via 231); and storing an electronic signal corresponding to said differential output signal. Transistors (N34, N35) when activated will pull the output approximately the same voltage (ground level).

Regarding claim 13-16, figure 7 of Takahashi (824) shows a method for storing electronic signals produced by a differential circuit comprising: applying clock (iclkb0) after pre-charging to bring the differential output terminal (the drain of N31 to a power supply voltage Vdd) and applying clock (iclkb3) to bring the differential output terminal (the source of N32 to a ground voltage).

Regarding claim 10, figure 7 shows a circuit comprising differential circuit comprising a differential domino circuit (P21, N21, P22, N22), the differential domino circuit and the differential sense latch (IN1, IN3, IN4, N33-N35) being coupled such that, in operation, differential output signals present on differential output terminals of the differential domino circuit cause a corresponding electronic signal to be stored in the differential sense latch.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (US Pat. 6,037,824).

Regarding claim 7, figure 7 of Takahashi (824) includes all the limitations of the present invention except for the limitation that the sense amplifier comprises an n-type sense amplifier. Figure 7 shows a p-type sense amplifier (P11-P13, N11- N13). However, it is well known the art that the n-type or the p-type sense amplifiers are exchangeable and are used depending on the type of supply voltages. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the n-type sense amplifier to conform to the "high level" input signals.

Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (5,982,689) further in view of Takahashi (6,037,824).

Regarding claims 17-20, figure 1 of Takahashi (689) show an integrated circuit (IC) comprising: a plurality of data paths, at least one of said data paths comprising: a differential circuit (not shown, outputting signals D and DB) and a differential sense latch (CELL, M31, M41, M11, M21), wherein said differential sense latch comprises a **differential sense circuit** (M31, M41, M11, M21) and a jam-latch (CELL) coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored

in said jam-latch; not disclosed is the **differential sense circuit** is coupled to said jam-latch in a push-pull configuration. Figure 7 of Takahashi (824) teaches a differential circuit (210, 220, 230), and a differential sense latch (IN1, IN3, IN4, N33-N35) wherein the differential sense circuit is coupled to the latch in a push-pull configuration for the purpose of supplying the latch with strong positive or negative- swing input signals. Therefore, it would have been obvious to those skilled in the art to implement the differential sense circuit differential circuit (210, 220, 230) of Takahashi (824) to differential sense latch (CELL, M31, M41, M11, M21) of Takahashi (689) for the purpose of supplying the jam-latch (CELL) with fully positive or negative- swing input signals and to improve the speed of differential sense latch circuit.

Regarding claims 21-24, the limitations "a processor", "a microprocessor", "a network processor and "a digital processor" are merely intended uses. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparartus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQF.2d 1647 (1987). Therefore, this limitation has not been given patentable weight.

Response to Arguments

In the Remarks, the applicant argues that Takahashi (824) "does not disclose a latch as claimed and described by Applicant". In claim 1, Applicant recites "a latch". Thus, any kind of latch can be used because Applicant does not describe the structure of the "a latch". Figure 7 of Takahashi (824) discloses a latch consisting of cross-coupled NAND gate" and "this latch configuration was disclosed by Applicant **as prior** art in the detailed description page 5, lines 4-12" and " the recited patent fails to meet each and every element and limitation of claim 1". In claim 1 Applicant recites **a latch** coupled to the differential amplifier for storing electronic signal. Figure 7 of Takahashi (824) shows a latch (233) coupled to the outputs of the differential sense circuit for storing electronic signal. This latch, consisting of cross-coupled NAND gates and a control signal (CLOCK CLK in figure 3 or iclkb3 in figure 7), is identical to the claimed latch described in the prior art in page 5, lines 4-12. Moreover, the electronic signal is stored in the latch circuit (233) when clock iclkb2 is inactive to transistors (N33, N34, N35). Thus, figure

7 of Takahashi discloses all the limitation of claim 1. When clock iclkb3 is active (low level), latch (233) is reset.

Applicant also states that there is no motivation to select the type of amplifier (n-type or p-type). It is old and well known for those skilled in the art that the selection of transistors for a circuit depends upon the polarities of the power supply as well as the polarities of the input signal (high or low). For instance, the prior art (figure 2) of the present application shows that the applicant has a choice for selection of amplifier types. If the current source of the amplifier is connected to a positive voltage and two pre-charge transistors are connected to the ground then the p-sense amplifier is used. If the current source of the amplifier is connected to the ground and two pre-charge transistors are connected to the positive voltage then the n-sense amplifier is used. Thus, changing the types of transistor for the circuit is not an invention and cannot be relied upon to distinguish over the prior art. Claim 7 depends upon claim 1. Thus it remains rejected under 103(a).

The method of claim 11 reads on the structure of claim 1. Thus it remains rejected under 102(e).

Applicant argues that "Takahashi (824) does not disclose a latch as claimed and described by Applicants". A mentioned above, Applicant never **describes** the structure of the latch of claim 1. Applicant is respectfully reminded that a claim is consider based on the recited elements and its language. The "a latch" of claim 1 is merely a latch, any kind of latch. In Takahashi (824), figure 1 discloses a jam latch (cell) comprising cross-coupled inverters. Figure 1 of Takahashi (689) shows all the limitations of claim 17 except for the well-known differential sense circuit that has the outputs coupled to the inputs (D, DB) of the circuit. Any differential sense circuit can be coupled to the circuit of Takahashi (689) to form the claimed "An integrated circuit". The advantage of the differential sense circuit of Takahashi (824) is that it has a push-pull output stage and it is well known in the art that the push-pull output accelerates the swing of the output signals. Thus, the differential sense circuit of Takahashi (824) has faster speed. Therefore, it is proper to utilize the differential sense circuit of Takahashi (824) as the well-known "not shown" differential sense circuit in figure 1 of Takahashi (689).

Allowable Subject Matter

Claims 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-9 are objected to because the prior art of record fails to teach or fairly suggest a differential sense amplifier comprising a first and second inverters having stacked n-devices as called for in claim 8.

Response to Arguments

In the Remarks, the applicant argues that Takahashi (824) "does not disclose a latch as claimed and described by Applicant". In claim 1, Applicant recites "a latch". Thus, any kind of latch can be used because Applicant does not describe the structure of the "a latch". Figure 7 of Takahashi (824) discloses a latch consisting of cross-coupled NAND gate" and "this latch configuration was disclosed by Applicant **as prior** art in the detailed description page 5, lines 4-12" and " the recited patent fails to meet each and every element and limitation of claim 1". In claim 1 Applicant recites **a latch** coupled to the differential amplifier for storing electronic signal. Figure 7 of Takahashi (824) shows a latch (233) coupled to the outputs of the differential sense circuit for storing electronic signal. This latch, consisting of cross-coupled NAND gates and a control signal (CLOCK CLK in figure 3 or iclkb3 in figure 7), is identical to the claimed latch described in the prior art in page 5, lines 4-12. Moreover, the electronic signal is stored in the latch circuit (233) when clock iclkb2 is inactive to transistors (N33, N34, N35). Thus, figure 7 of Takahashi discloses all the limitation of claim 1. When clock iclkb3 is active (low level), latch (233) is reset.

Applicant also states that there is no motivation to select the type of amplifier (n-type or p-type). It is old and well known for those skilled in the art that the selection of transistors for a circuit depends upon the polarities of the power supply as well as the polarities of the input signal (high or low). For instance, the prior art (figure 2) of the present application shows that the applicant has a choice for selection of amplifier types. If the current source of the amplifier is connected to a positive voltage and two pre-charge transistors are connected to the ground then the p-sense amplifier is used. If the current source of the amplifier is connected to the ground and two pre-charge transistors are connected to the positive voltage then the n-sense amplifier is

used. Thus, changing the types of transistor for the circuit is not an invention and cannot be relied upon to distinguish over the prior art. Claim 7 depends upon claim 1. Thus it remains rejected under 103(a).

The method of claim 11 reads on the structure of claim 1. Thus it remains rejected under 102(e).

Applicant argues that Takahashi (824) does not disclose a latch as claimed and described by Applicants". A mentioned above, Applicant never **describes** the structure of the latch of claim 1. Applicant is respectfully reminded that a claim is consider based on the recited elements and its language. The "a latch" of claim 1 is merely a latch, any kind of latch. In Takahashi (824), figure 1 discloses a jam latch (cell) comprising cross-coupled inverters. Figure 1 of Takahashi (689) shows all the limitations of claim 17 except for the well-known differential sense circuit that has the outputs coupled to the inputs (D, DB) of the circuit. Any differential sense circuit can be coupled to the circuit of Takahashi (689) to form the claimed "An integrated circuit". The advantage of the differential sense circuit of Takahashi (824) is that it has a push-pull output stage and it is well known in the art that the push-pull output accelerates the swing of the output signals. Thus, the differential sense circuit of Takahashi (824) has faster speed. Therefore, it is proper to utilize the differential sense circuit of Takahashi (824) as the well-known "not shown" differential sense circuit in figure 1 of Takahashi (689).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
04-12-02

TUAN T. LAM
PRIMARY EXAMINER